REMARKS

Claims 1-29 are pending in the present application. Claims 1, 2, 12, 13, 23, and 24 were amended. Reconsideration of the claims is respectfully requested.

35 U.S.C. § 102, Anticipation

The Examiner has rejected Claims 1,2,6-8, 11 and 17 under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 5,995,306, to Contreras et al. This rejection is respectfully traversed.

The Examiner has rejected Claims 13,14, and 19-22 under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 6,122,124, to Fasen et al. This rejection is also respectfully traversed.

35 U.S.C. § 103, Obviousness

The Examiner has rejected Claims 9, 10, 12, 18 and 23-28 under 35 U.S.C. § 103 as being obvious in view of the Contreras et al. patent combined with the Fasen et al patent. Claims 3-5 have been rejected as being obvious in view of Contreras combined with a reference of Abe (Derwent Acc. No. 1992-167403). Claims 15, 16 and 29 have been rejected as being obvious in view of Fasen respectively combined with U.S. Patent Nos. 6,028,488 (to Landman et al.); 6,389,090 (to Forten et al); and 6,075,666 (to Gillingham et al.). All of the obviousness rejections are respectfully transverse.

Claim 1, as now amended, recites the step of "reading successive reference regions on the moving storage medium to derive a timing-signal having a frequency that varies directly with variations in the speed of the moving storage medium". This step is disclosed in Applicants' specification, such as at page 8, lines 27-29 and page 9, lines 1-3, wherein it is stated that;

> As magnetic tape **108** moves in relation to read/write head assembly **106**, read/write head assembly **106** reads a timing signal **116** from reference regions written on magnetic tape **108**. This timing signal will increase or decrease in frequency, in direct relation to the change in tape speed.

Amended Claim 1 further recites the step of "processing the timing signal to provide a clock signal having a frequency that is a function of the timing signal, and thereby represents the speed of the storage medium". This step is disclosed in **Figure 7** of Applicants' drawings, together with related teachings of the specification. **Figure 7** shows that the clock signal f_{clk} is in fact equal to a reference frequency f_{ref} multiplied by an integer N. The application at page 15, lines 7-8, states that "reference frequency **702** is the processed timing signal".

Amended Claim 1 further recites the step of "using the clock signal to determine the rate for writing data to the moving storage medium, so that said rate is proportional to the speed of the moving storage medium". Important features of this step are disclosed in Applicants' specification, for example, at page 9, lines 4-6, wherein it is stated that "Clock generation circuitry **118** processes timing signal **116** to generate a clock signal **102** that may be used to time the reading and writing of data **104**".

By providing the recitation of Claim 1 as now amended, directed to a method of establishing a data transfer rate between a moving storage and a read/write device, Applicants achieve an important objective in making their invention. As stated in their application at page 4, lines 9-12, this objective is to use the clock signal "to time reads and writes to and from the medium so that the medium may be read or written to at any speed".

Applicants consider that Claim 1 as now amended patentably distinguishes over the cited Contreras reference, particularly in reciting, in the over-all combination of Claim 1, the step of using the clock signal to determine the rate for writing data to the moving storage medium. The purpose and principal focus of Contreras is set forth, for example, at column 3, lines 5-13;

> Method and apparatus are provided for re-recording of a frame on magnetic tape when a first recording of the frame is determined to be defective. A frame whose first recording is defective is re-recorded at a spare or reserved location on the tape. The reserved location is dedicated to re-recoding of frames, and otherwise cannot have data stored therein. The tape contains a defect map frame with the reserved location whereat the frame is re-recorded.

The Contreras et al. reference, at column 9, lines 25-31, teaches that a servo sense TS signal, buried or embedded in tape 32, is processed to obtain a servo clock signal TS_c:

> Servo position recovery circuit 176 serves to process the buried servo sense TS signal on six of the eight channels in order to determine whether head unit 100 is properly following tracks recorded on tape 32. Servo clock recovery circuit 174 serves to process the buried servo sense TS signal on two of the eight channels in order to obtain a servo clock signal TS.

In citing the Contreras reference against Applicants' original Claim 1, the Examiner stated the following in regard to an element of such claim:

> Writing of data to the moving storage medium at a rate proportional to the speed of the moving medium (Col. 39, L.33-38 and Col. 41, L. 42 to Col 42, L.6).
>
> Office Action dated July 29, 2004, page 3

The sections referred to by the Examiner in the above statement appear to be the teachings of Contreras that are most relevant to Applicants' Claim 1. These sections pertain to tape speed control and are associated with FIG. 36A of the Contreras drawings. At column 39, lines 33-39, Contreras et al. states the following:

> Conventional drives use external reference, e.g., crystal oscillators, to control linear speed of tape and the rate of recording of data on the tape. As seen hereinafter, the linear speed of tape 32 is controlled by the data transfer rate to and from the host as reflected, e.g., by a detected "buffer level" of buffer memory 116. The rate of recording of user data is, in turn, dependent upon the linear speed of tape 32 as detected with reference to the clocking signal TS. (Emphasis added.)

In the above statement, Contreras emphasizes that tape speed is controlled by the data transfer rate. This statement of Contreras clearly teaches away from the Claim 1 recitation of using a clock signal, representing storage medium speed, to determine or control, and not be controlled by, data writing rates. Accordingly, an essential teaching of Claim 1 is in direct opposition to the teachings of the Contreras et al. reference.

The above teachings of Contreras are further emphasized, such as at column 39, lines 57-61 and column 40, lines 7-8. Contreras states the following at these sections:

> FIG. **36A** shows a first embodiment of tape speed controller **133**. An initial desired tape speed value (in, e.g., inches per second) is applied to tape speed controller **133** as represented by input **133-1**. Adder **133-2** adds an adjustment value (represented by input line **133-3**).
>
> The adjustment value represented by input line **133-3** depends on the amount of user data in buffer memory **116**.

The above statements demonstrate that Contreras teaches adjusting tape speed control according to the contents of a data buffer, which reflects data transfer rate as indicated above. This teaching clearly departs from essential features recited by Applicants' Claim 1.

Applicants consider that neither the Fasen et al. reference nor any of the other references cited by the Examiner, either alone or in any combination with one another or with Contreras, overcomes the deficiencies of Contreras discussed above in regard to Applicants' Claim 1.

Claim 2 depends from Claim 1, and is considered to patentably distinguish over the art for the same reasons giving in support thereof. In addition, Claim 2 is considered to distinguish over the art, including the cited references, particularly in reciting reference regions that extend in a second direction, that is perpendicular to a first direction of storage medium movement, and in further reciting that respective reference regions are interleaved with timing-based servo regions that extend along diagonals with respect to the first and second directions. These features are shown in both Figures 3 and 4 of Applicants' drawings. These features are also disclosed in the specification, such as at page 12, lines 11-21, wherein it is stated that:

> As the references regions pass by read/write head assembly **106** and are read, a timing signal (**116** in **Figure 1**) is produced with a frequency that matches the frequency at which the reference regions are read. A vertical reference region, such as reference region **308** is preferable to diagonal regions **304** and **306** for generating a timing signal. This is because the timing signal read from a vertical reference region

> does not change in frequency, phase, or pulse width as the read/write head assembly moves up or down, unlike a timing-based servo signal.

It is clear from the above statement that the vertically extending reference regions 308 disclosed by Applicants are much more useful for Applicants' purposes than the diagonal regions 304 and 306 that are used for timing-based servo signals. The vertical reference regions are better for providing timing signals, which is the only requirement needed for Applicants' invention. By interleaving the reference regions with the diagonal servo regions, Applicants disclose an arrangement that has all the capabilities provided by both types of regions.

Applicants consider that none of the references cited by the Examiner, nor any combination thereof, either shows or suggests the combination of features recited by Applicants' amended Claim 2. Clearly, the Contreras patent fails to show or in any way suggest such features. The Fasen reference, as demonstrated by Figure 2 thereof, is limited to diagonal features, and would have no need for the combination of features recited by Applicants' Claim 2.

Claims 3-11 respectively depend from Claim 1, and are each considered to parentably distinguish over the art for the same reasons giving in support thereof.

Claim 12 depends from Claims 1 and 2, and is considered to patentably distinguish over the art for the same reasons given in support thereof. In addition, Claim 12 is considered to distinguish over the cited art in reciting reference regions that are respectively interleaved with timing-based servo regions located on the moving storage medium, wherein the reference regions are being adapted to provide information representing only the speed of the storage medium along the first direction, and the timing-based servo regions are adapted to provide information representing the position of the storage medium along a second direction perpendicular to the first direction. These features are disclosed in the application, such as at page 12, lines 11-21, set forth above, and at page 11, lines 7-19, wherein it is stated that:

> For example, if servo read head **206** is misaligned, so that it skims the tops of regions **208, 210,** and **212,** regions **208** and **212** will appear close together, while regions **212** and **210** will appear far apart. Conversely, if servo read head **206** is misaligned in the opposite direction (down), then regions **208** and **212** will appear far apart with regions **212**

> and **210** appearing close together. With servo read head **210** aligned in the center of this band, regions **208, 212,** and **210** will appear equally spaced. Thus, servo control **124** can keep read/write head assembly **106** aligned by adjusting the alignment of read/write head assembly **106** to keep the regions properly spaced.

Applicants consider that none of the references cited by the Examiner, or any combination thereof, either shows or suggests the combination of features recited by Applicants' amended Claim 12. Applicants consider that neither the Contreras nor the Fasen reference, in particular, would have any need for the reference regions of Claim 12, in addition to the timing-based servo regions thereof.

Claim 13 has been amended to enhance clarity. Claim 13 has been further amended to recite that the output of the voltage-controlled oscillator is coupled to the second input of the phase detector, to form a phase locked loop wherein the voltage-controlled oscillator is locked to the timing signal to generate a signal representing a data transfer rate. This feature is disclosed in the application, such as at page 16, lines 6-12, wherein it is stated that:

> Since both inputs to phase detector **704** equal f_{clk}/N, any shift in one of these frequencies will be detected by phase detector **704** and feed through charge pump **706** to voltage controlled oscillator **714**. This results in f_{clk} being adjusted to bring it back into sync to a value $N*f_{ref}$. This is sync condition is known as being "in lock," hence the name phase-locked loop.

Claim 13 is considered to distinguish over the prior art, including the Fasen et al. reference, particularly in reciting, in the over-all combination of Claim 13, coupling the output of the phase detector into the control input of the voltage-controlled oscillator, and the output of the voltage-controlled oscillator to the second input of the phase detector, to form a phase locked loop wherein the voltage-controlled oscillator is locked to the timing signal to generate a signal representing a data transfer rate.

In the Fasen reference, a principal teaching is the significant disadvantage of using a phase locked loop (PLL) to generate a clock signal for use in connection with data exchange in a magnetic storage medium. At col. 3, lines 37-57, Fasen states:

A disadvantage of this phase locked loop approach is in the fact that the frequency generated by the analog voltage controlled oscillator as a function of the control voltage is unpredictable over temperature, power supply voltage and part to part variations. Due to this unpredictability, a loop is locked using a phase/frequency comparator to adjust the voltage controlled oscillator control voltage until the voltage controlled oscillator phase and frequency matches the desired phase and frequency.

This feedback requirement makes holding the frequency of the voltage controlled oscillator constant over long servo dropouts difficult. If the phase/frequency comparator simply stops receiving pulses from the tape servo code, the voltage controlled oscillator will drift in frequency from the last good data. Methods to switch the phase locked loop into a hold mode are also prone to offsets and drift in the held frequency. Also, if an ATS range greater than the current range was required, the analog voltage controlled oscillator in the phase locked loop would need to have multiple ranges. This would require spaces left on the tape to allow the phase locked loop to settle into the new range.

Fasen further teaches that expressly in view of the disadvantages of a PLL, a digitally controlled oscillator is to be used to define a clock. This teaching is set forth in Fasen at col. 8, lines 54-59:

> A multiple phase clock generator can also be employed in a tracking clock used to write data to the tape such that data bits written on the tape are evenly spaced on the tape regardless of tape speed. To avoid the analog circuit problems discussed above in the Background of the Invention, a digitally controlled oscillator (DCO) **110** is employed in the ASIC **49** (FIG. **3**) to define a tracking clock **162**. The tracking clock **162** is used in connection with writing data to the tape **34**.

Thus, Fasen clearly and explicitly teaches against use of a phase locked loop as recited in Applicants' Claim 13. The PLL 164 of Fasen, as shown in FIG. 3 thereof, is only used to control an analog filter. The PLL 166 is used only to multiply clock signal 164. These limited uses are set forth in Fasen at col. 9, lines 3-22:

> The ASCI **49** further includes an analog filter control PLL **164**. The tape drives **14** and **16** respectively include an analog filter **174** which is a readback filter which filters the readback signal from the servo read element **39**. The bandwidth of the analog filter **174** tracks the speed of the tape **34**. More particularly, the analog filter control PLL **164** causes the bandwidth of the analog filter **174** to track the input clock to the PLL **164**. The input clock to the PLL **164** is the tracking clock **162**.

> The tape drives **14** and **16** further respectively include a data write clock generating PLL **166** having an input coupled to the tracking clock **162**. The tape drives **14** and **16** further respectively include a read/write system **168** having a write clock coupled to the data write clock generating PLL **166** and to the data write element **170**. The read/write system **168** further has an analog filter coupled to the data write clock generating PLL **166** and to the data read element **172**. The data write clock generating PLL **166** multiplies the tracking clock **162** to a frequency appropriate for the write clock of the read/write system **168**.

Moreover, the Fasen reference further emphasizes that the term "locked" does not mean a circuit operating in a locked condition, as is recited and required by Applicants' Claim 13. This teaching of Fasen is set forth at col. 3, lines 28-37:

> The term "phase locked loop" as used herein are meant to describe physical structure, not a state of operation. The term "locked" in the phrase "phase locked loop" does not imply that the circuitry is operating or functioning in a locked condition. Thus, as used herein, "locked" is a term for assisting definition of a particular circuit configuration and is not meant to imply a required state of operation for the circuit.

Applicants consider that in view of the above statements, the prior art as exemplified by the Fasen reference expressly teaches away from key features of Applicants' Claim 13. Applicants consider further that in view of the clear and repeatedly emphasized teachings of Fasen, those of skill in the art would have no reason to combine teachings of any other cited references, such as the Abe reference, with Fasen in regard to Applicants' Claim 13. To the contrary, in view of the teachings of Fasen, those of skill in the art would be motivated against any such combinations. Phase locked loops are, of course, used widely in many different areas of application. The Abe reference refers to a phase locked loop, but in no way discloses or implies that its teachings pertain to a moving storage medium.

Claims 14-22 respectively depend from Claim 13, and are each considered to patentably distinguish over the art for the same reasons given in support thereof.

Claim 23, as now amended, is considered to patentably distinguish over the prior art, particularly in reciting reference regions that are adapted to provide information representing only the speed of the recording surface along a first direction, and timing-based servo regions that are adapted to provide information representing the position of

the recoding surface along a second direction perpendicular to the first direction. Such recitation is considered to distinguish over the art for the same reasons set forth above in regard to Claim 12.

Claims 24-29 respectively depend from Claim 23, and are each considered to patentably distinguish over the art for the same reasons given in support thereof.

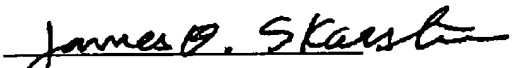
Conclusion

It is respectfully urged that the subject application is patentable over the cited references and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: October 29, 2004

Respectfully submitted,



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